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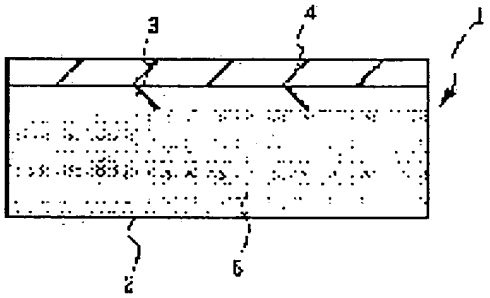
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a gettering method concerning a clad-type SOI (silicon on insulator) wafer.
SOLUTION: A BOX 3 is formed on a semiconductor supporting substrate 2, a surface silicon layer 4 is formed on the BOX 3 and a semiconductor integrated circuit chip is formed on the surface silicon layer 4. Oxygen deposited substances 5 are formed in the whole semiconductor substrate 2 as a gettering region. Impurities such as heavy metal atoms, etc. existing in the surface silicon layer 4 are trapped by the oxygen depoited substances 5 through the BOX 3 to reduce the impurity concentration of the surface silicon layer 4. Further, a polycrystalline silicon film, a silicon nitride film or a mechanically damaged layer which is formed on the rear of the semiconductor supporting substrate 2 may be used as the gettering region.



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CLAIMS

[Claim(s)]

[Claim 1] Semi-conductor accumulation time equipment which is semiconductor integrated circuit equipment with which the semiconductor integrated circuit component was formed in said semi-conductor thin film layer of the substrate for semiconductor integrated circuits which has a semi-conductor support substrate, the insulating layer prepared on said semi-conductor support substrate, and the semi-conductor thin film layer prepared on said insulating layer, and is characterized by establishing a gettering field in said semi-conductor support substrate.

[Claim 2] It is semiconductor integrated circuit equipment which is semiconductor integrated circuit equipment according to claim 1, and is characterized by said gettering field consisting of an oxygen sludge distributed over said whole semi-conductor support substrate.

[Claim 3] It is semiconductor integrated circuit equipment which is semiconductor integrated circuit equipment according to claim 1, and is characterized by said gettering field consisting of an impurity diffused layer by which it was formed in the interface of said semi-conductor support substrate and said insulating layer, and Lynn (P) was introduced into high concentration.

[Claim 4] It is semiconductor integrated circuit equipment characterized by being semiconductor integrated circuit equipment according to claim 1, and forming said gettering field of the thin film or stress generating field established in the rear face of said semi-conductor support substrate which uses said semi-conductor thin film layer as a front face.

[Claim 5] It is semiconductor integrated circuit equipment which is semiconductor integrated circuit equipment according to claim 1 or 4, and is characterized by said thin film being a polish recon thin film.

[Claim 6] It is semiconductor integrated circuit equipment characterized by being what formed of a stress difference with the silicon nitride film which is semiconductor integrated circuit equipment according to claim 1 or 4, and was formed in the surface roughening processing by the collision of the particle by which said stress generating field was injected by said rear face, or said rear face.

[Claim 7] It has a semiconductor integrated circuit component in the semi-conductor thin film layer prepared on the insulating layer on a semi-conductor support substrate. It is the manufacture approach of semiconductor integrated circuit equipment of having a gettering field in said semi-conductor support substrate. (a) The process which forms a gettering field in the 1st semi-conductor substrate used as said semi-conductor support substrate, (b) Said 2nd semi-conductor substrate with which silicon oxide was formed in the front face of the 2nd semi-conductor substrate used as said semi-conductor thin film layer, and said silicon oxide was formed, The manufacture approach of semiconductor integrated circuit equipment of having the process which grinds the part which starts said 2nd semi-conductor substrate among the process which joins the 1st [said] semi-conductor substrate which has said gettering field, and forms a junction substrate, and the (c) aforementioned junction substrate, and forms said semi-conductor thin film layer.

[Claim 8] It is the manufacture approach of semiconductor integrated circuit equipment according to claim 7. Said gettering field By being formed by heat-treating said 1st semi-

conductor substrate, and carrying out the ion implantation of Lynn (P) to the 1st configuration which consists of an oxygen sludge distributed over said whole semi-conductor support substrate, and said 1st semi-conductor substrate Or the manufacture approach of the semiconductor integrated circuit equipment characterized by being which configuration of 2nd configuration ** which consists of an impurity diffused layer which was formed by introducing Lynn (P) by thermal diffusion, and was formed in the interface of said semi-conductor support substrate and said insulating layer.

[Claim 9] It has a semiconductor integrated circuit component in the semi-conductor thin film layer prepared on the insulating layer on a semi-conductor support substrate. It is the manufacture approach of semiconductor integrated circuit equipment of having a gettering field in said semi-conductor support substrate. (a) Said 2nd semi-conductor substrate with which silicon oxide was formed in the front face of the 2nd semi-conductor substrate used as said semi-conductor thin film layer, and said silicon oxide was formed, The process which joins the 1st semi-conductor substrate used as said semi-conductor support substrate, and forms a junction substrate, (b) The manufacture approach of semiconductor integrated circuit equipment of having the process which grinds the part which starts said 2nd semi-conductor substrate among the process which forms a gettering field in said both-sides [of said junction substrate], or 1st semi-conductor substrate side, and the (c) aforementioned junction substrate, and forms said semi-conductor thin film layer.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention is applied to the gettering of the lamination SOI (Silicon on Insulator) wafer used for manufacture of a high speed and a low power LSI about semiconductor integrated circuit equipment and its manufacturing technology, and relates to an effective technique.

[0002]

[Description of the Prior Art] The SOI technique which can make small the junction capacitance of a component and a semi-conductor substrate for the purpose of application to a high speed and a low power LSI attracts attention.

[0003] The wafer which has SOI structure, i.e., a SOI wafer, is indicated in detail by November 30, Showa 59, Ohm-Sha Issue, an "LSI handbook", and p388-p390, for example. It explains briefly below.

[0004] Generally the SOI wafer has constituted 3 layer structure. The maximum upper layer (a surface silicon layer is called below) is a single-crystal-silicon layer with a thickness of 0.1 micrometers - several micrometers, and a semiconductor integrated circuit component is formed here. As an interlayer, it is the embedding SiO2 of 100nm of thickness numbers. It has the film (Following BOX is called) and has a silicon substrate in the lowest layer.

[0005] Also in such a SOI wafer, the technique of carrying out gettering of the impurities, such as a metal atom contained in the surface silicon layer which serves as a field in which a semiconductor integrated circuit component is formed like a silicon wafer, or a defect, and raising the engine performance of a semiconductor integrated circuit component is required.

[0006] There is JP,6-61235,A as a gettering technique in a SOI wafer. That is, gettering layers, such as a high concentration in plastic layer and a polycrystalline silicon layer, are prepared in right above [of the embedding oxide film of the substrate for semiconductor integrated circuits of SOI structure] using a wafer lamination technique for the purpose of offering the semiconductor integrated circuit equipment and its manufacture approach of the SOI structure in which the high electric reliability of a device and the high yield are possible.

[0007] Moreover, since it was considered that a heavy-metal atom hardly penetrated BOX conventionally, to the SOI wafer, it was thought that the conventional in thorin chic gettering method and the IKUSU thorin chic gettering method were inapplicable, and the effective gettering method was not proposed.

[0008] However, in J.Electrochem.Soc. besides J.Jablonski, the 142nd volume ** No. 6 2059 pages, and June, 1995, it is reported from the experiment using a SIMOX wafer that a heavy-metal atom penetrates BOX of 100nm of thickness numbers, and the gettering method for a SIMOX wafer is proposed from it. If this proposal is explained briefly, the getter of the heavy-metal atom in a surface silicon layer will be carried out to the ion-implantation damage layer directly under BOX.

[0009]

[Problem(s) to be Solved by the Invention] As for the technique shown in above-mentioned JP,6-61235,A, preparing a gettering layer between the surface silicon layers and BOX(s)

which have the thickness of 0.1 micrometers - several micrometers, and preparing a gettering layer in the lower part of such a thin surface silicon layer is accompanied by the difficulty on a process.

[0010] Moreover, although the technique shown in reference besides said J.Jablonski prepares a gettering layer in the BOX lower part, since a gettering layer is what is formed as a damage layer of an ion implantation through a surface silicon layer, it is difficult to keep high the quality of the surface silicon layer which influences the engine performance of a semiconductor integrated circuit component after BOX formation.

[0011] The purpose of this invention is to offer semiconductor integrated circuit equipment equipped with the gettering layer which has high gettering capacity.

[0012] Other purposes of this invention are to offer the simple manufacture approach of such semiconductor integrated circuit equipment.

[0013] The purpose of further others of this invention carries out gettering of the impurity by the gettering layer, and is to improve the engine performance of semiconductor integrated circuit equipment.

[0014] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.

[0015]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.

[0016] (1) The semiconductor integrated circuit equipment of this invention is semiconductor integrated circuit equipment with which the semiconductor integrated circuit component was formed in the semi-conductor thin film layer of the substrate for semiconductor integrated circuits which has the insulating layer prepared on the semi-conductor support substrate and the semi-conductor support substrate, and the semi-conductor thin film layer prepared on the insulating layer, and establishes a gettering field in a semi-conductor support substrate.

[0017] Since the gettering field was established in the semi-conductor support substrate of the substrate for semiconductor integrated circuits illustrated by SOI according to such semiconductor integrated circuit equipment, it is not necessary to establish a gettering field in the semi-conductor thin film layer prepared on the insulating layer, and the engine performance of the semiconductor integrated circuit component formed in the semi-conductor thin film layer can be improved.

[0018] That is, an effective gettering field can be formed by the easy manufacture approach by adopting the configuration which prepares a gettering field as the conventional semi-conductor support substrate instead of a configuration which establishes a gettering field in the interface of the semi-conductor thin film layer and insulating layer from which a production process becomes complicated.

[0019] (2) The semiconductor integrated circuit equipment of this invention is semiconductor integrated circuit equipment of the aforementioned (1) publication, and uses a gettering field as the oxygen sludge distributed over the whole semi-conductor support substrate.

[0020] According to such semiconductor integrated circuit equipment, the engine performance of a semiconductor integrated circuit component can be improved by using a gettering field as the oxygen sludge distributed over the whole semi-conductor support substrate. That is, gettering of the impurities, such as a metal which exists in a semi-

conductor thin film layer, or a defect, can be carried out to the distortion field formed with the oxygen sludge, and the impurity in a semi-conductor thin film layer can be reduced.

[0021] Moreover, by establishing the gettering field which consists of an oxygen sludge in the semi-conductor support substrate instead of a semi-conductor thin film layer, it dissociates and a semi-conductor thin film layer can form a gettering field. Therefore, the hysteresis of annealing temperature can be devised, it is not necessary to form a denuded zone in a semi-conductor thin film layer, and a production process can be simplified.

[0022] (3) Lynn which the semiconductor integrated circuit equipment of this invention is semiconductor integrated circuit equipment of the aforementioned (1) publication, and was formed in the interface of a semi-conductor support substrate and an insulating layer in the gettering field -- (P) considers as the impurity diffused layer introduced into high concentration.

[0023] Since according to such semiconductor integrated circuit equipment the engine performance of a semiconductor integrated circuit component can be improved and the impurity diffused layer which can simplify a production process and into which further high-concentration Lynn (P) was introduced was prepared, gettering of the metal impurity can be carried out according to the chemical operation by increase of ****** of a metallic element.

[0024] (4) The semiconductor integrated circuit equipment of this invention is semiconductor integrated circuit equipment of the aforementioned (1) publication, and forms a gettering field by the thin film or stress generating field established in the rear face of the semi-conductor support substrate which uses a semi-conductor thin film layer as a front face.

[0025] Since it forms by the thin film or stress generating field in which the gettering field was established at the rear face of a semi-conductor support substrate according to such semiconductor integrated circuit equipment, the engine performance of a semiconductor integrated circuit component can be improved, and a production process can be simplified. That is, since it is the structure which added the gettering field to the substrate for semiconductor integrated circuits which does not have a gettering field, a gettering field can be formed comparatively freely in the phase of the arbitration of the production process of semiconductor integrated circuit equipment. Thereby, it becomes easy to attain optimization of the whole production process of semiconductor integrated circuit equipment.

[0026] (5) The semiconductor integrated circuit equipment of this invention is semiconductor integrated circuit equipment the above (1) or given in (4), and uses a thin film as a polish recon thin film.

[0027] Since the thin film which is a gettering field is used as a polish recon thin film according to such semiconductor integrated circuit equipment, gettering of a metal impurity can be performed effectively and the engine performance of semiconductor integrated circuit equipment can be improved.

[0028] That is, the gettering capacity of the metal impurity not only by an operation of the space [distortion] by the stress formed in the interface of the polish recon thin film and the rear face of a semi-conductor support substrate but operation of the grain boundary of the crystal defect which exists in a polish recon thin film, especially the silicon grain which constitutes a polish recon thin film can be increased by making a polish recon thin film into a gettering field.

[0029] (6) The semiconductor integrated circuit equipment of this invention is semiconductor integrated circuit equipment the above (1) or given in (4), and forms a stress generating field by the stress difference with the silicon nitride film formed in the surface roughening processing by the collision of the particle injected by the rear face, or a rear face.

[0030] Since the stress generating field is formed by the stress difference with the silicon nitride film formed in the surface roughening processing by the collision of the particle injected by the rear face, or a rear face according to such semiconductor integrated circuit equipment, gettering of a metal impurity can be performed effectively and the engine performance of semiconductor integrated circuit equipment can be improved.

[0031] That is, the surface roughening processing by the collision of the particle to the rear face of a semi-conductor support substrate or formation of a silicon nitride film makes that field processed or formed generate big stress, and formation of the space [distortion] by this stress performs gettering of a metal impurity very effectively.

[0032] (7) The manufacture approach of the semiconductor integrated circuit equipment of this invention It has a semiconductor integrated circuit component in the semi-conductor thin film layer prepared on the insulating layer on a semi-conductor support substrate. It is the manufacture approach of semiconductor integrated circuit equipment of having a gettering field in a semi-conductor support substrate. (a) The process which forms a gettering field in the 1st semi-conductor substrate used as a semi-conductor support substrate, (b) Silicon oxide is formed in the front face of the 2nd semi-conductor substrate used as a semi-conductor thin film layer. It has the process which joins the 2nd semi-conductor substrate in which silicon oxide was formed, and the 1st semi-conductor substrate which has a gettering field, and forms a junction substrate, and the process which grinds the part concerning the semi-conductor substrate of [2nd] the (c) junction substrates, and forms a semi-conductor thin film layer.

[0033] In order according to the manufacture approach of such semiconductor integrated circuit equipment to form a gettering field in the 1st semi-conductor substrate and to form the substrate for semiconductor integrated circuits by sticking with the 2nd semi-conductor substrate created independently, the semi-conductor thin film layer in which a semiconductor integrated circuit component is formed of the production process of a gettering field is not influenced. Consequently, it can hold good, without degrading the quality of the semi-conductor thin film layer which influences the engine performance of a semiconductor integrated circuit component by the production process of a gettering field.

[0034] (8) The manufacture approach of the semiconductor integrated circuit equipment of this invention It is the manufacture approach of the semiconductor integrated circuit equipment the aforementioned (7) publication. A gettering field The oxygen sludge distributed over the whole semi-conductor support substrate formed by heat-treating the 1st semi-conductor substrate, Or let Lynn (P) be either of the impurity diffused layer **s which were formed an ion implantation or by carrying out thermal diffusion, and were formed at the interface of a semi-conductor support substrate and an insulating layer at the 1st semi-conductor substrate.

[0035] According to the manufacture approach of such semiconductor integrated circuit equipment, an oxygen sludge or an impurity diffused layer can optimize an oxygen sludge or the process conditions of manufacture of an impurity diffused layer, without being able to manufacture apart from the 2nd semi-conductor substrate containing the semi-

conductor thin film layer which influences the engine performance of a semiconductor integrated circuit component, and taking into consideration physical-properties change of the 2nd semi-conductor substrate.

[0036] (9) The manufacture approach of the semiconductor integrated circuit equipment of this invention It has a semiconductor integrated circuit component in the semi-conductor thin film layer prepared on the insulating layer on a semi-conductor support substrate. It is the manufacture approach of semiconductor integrated circuit equipment of having a gettering field in a semi-conductor support substrate. (a) Silicon oxide is formed in the front face of the 2nd semi-conductor substrate used as a semi-conductor thin film layer. The process which joins the 1st semi-conductor substrate used as the 2nd semi-conductor substrate with which silicon oxide was formed, and a semi-conductor support substrate, and forms a junction substrate, (b) The part which starts the 2nd semi-conductor substrate among the process which forms a gettering field in a both-sides [of a junction substrate] or 1st semi-conductor substrate side, and (c) junction substrate is ground, and it has the process which forms a semi-conductor thin film layer.

[0037] Since according to the manufacture approach of such semiconductor integrated circuit equipment a gettering field is formed in the both sides or the 1st semi-conductor substrate side after sticking the 1st semi-conductor substrate and the 2nd semi-conductor substrate, a production process can be simplified. namely, in forming a thin film in a 1st semi-conductor substrate side, i.e., the rear face of the substrate for semiconductor integrated circuit components, and making this into a gettering field Rather than it adopts the 2nd semi-conductor substrate and the process to stick after establishing a gettering field in the 1st semi-conductor substrate beforehand Since the direction in which a gettering field is established does not need to remove before lamination the contamination generated at the time of thin film formation after sticking the 1st and 2nd semi-conductor substrates, a process can be simplified and it is advantageous.

[0038]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing.

[0039] (Gestalt 1 of operation) Drawing 1 is the important section sectional view having shown an example of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[0040] The semiconductor integrated circuit equipment 1 of the gestalt 1 of this operation does not have the SOI structure which consists of a surface silicon layer 4 which is a semi-conductor thin film layer formed on BOX3 and BOX3 which are the insulating layer formed on the semi-conductor support substrate 2 and the semi-conductor support substrate 2, and although not illustrated in the surface silicon layer 4, the semiconductor integrated circuit component is formed.

[0041] The semi-conductor support substrate 2 has the oxygen sludge 5 used as the site of gettering. the oxygen sludge 5 -- the whole of the semi-conductor support substrate 2 -- almost -- homogeneity -- being distributed -- the consistency -- 104-106 An individual / cm3 it is .

[0042] According to such semiconductor integrated circuit equipment 1, gettering of the impurity which exists in the surface silicon layer 4 can be carried out with the oxygen sludge 5 which exists in the semi-conductor support substrate 2 through BOX3. The engine performance of the semiconductor integrated circuit component formed in the

surface silicon layer 4 can be improved by this, and high-performance-izing of semiconductor integrated circuit equipment 1 and improvement in the yield can be aimed at.

[0043] Next, the manufacture approach of the semiconductor integrated circuit equipment 1 of the gestalt 1 this operation is explained according to drawing 2 - drawing 7 .

[0044] First, the silicon wafer 6 which is the 1st semi-conductor substrate is prepared (drawing 2). A silicon wafer 6 serves as the semi-conductor support substrate 2.

[0045] The crystal property of a silicon wafer 6 can be made into 550 micrometers in field bearing (100), electric conduction form N type, resistivity 10 ohm-cm, oxygen density lx1018 atom / cm3, the diameter of 125mm, and thickness.

[0046] Next, the precipitation-of-oxygen nucleus 7 is formed in the interior of a wafer by annealing a silicon wafer 6 (drawing 3 R> 3). Annealing conditions can make temperature 750 degrees C among N2 ambient atmosphere, and can make the processing time 5 hours.

[0047] Next, the silicon wafer 8 which is the 2nd semi-conductor substrate is prepared (drawing 4). A silicon wafer 8 turns into a near bond wafer with which the component of a SOI wafer is formed.

[0048] The crystal property of a silicon wafer 8 can be made into 550 micrometers in field bearing (100), electric conduction form N type, resistivity 10 ohm-cm, oxygen density 8x1017 atom / cm3, the diameter of 125mm, and thickness.

[0049] Next, a silicon wafer 8 is oxidized thermally, BOX3 with a thickness of 500nm is formed in a front face, and it considers as the bond wafer 9 (drawing 5).

[0050] Next, after making a mirror plane side counter mutually and piling up a silicon wafer 6 and the bond wafer 9, while performing 1050 degrees C and annealing of 3 hours in N2 ambient atmosphere and pasting both up firmly, the precipitation-of-oxygen nucleus 7 formed in the silicon wafer 6 is grown up into the oxygen sludge 10 (drawing 6). Thereby, the lamination wafer 11 is obtained.

[0051] next, the field by the side of the bond wafer 9 of the lamination wafer 11 -- up to thickness thicker [10 micrometers of numbers] than the thickness of the surface silicon layer 4 predetermined with a surface grinder -- removing -- after that -- the chemical mechanical grinding method -- the thickness (for example, 2 micrometers) of the predetermined surface silicon layer 4 -- until -- it grinds (drawing 7). Thus, the substrate for semiconductor integrated circuits which has the oxygen sludge 10 used as a gettering site is formed into the semi-conductor support substrate 2 under BOX3.

[0052] Finally a semiconductor integrated circuit component is formed in the front face of the surface silicon layer 4 using a well-known technique, and semiconductor integrated circuit equipment 1 is completed.

[0053] According to the manufacture approach of such semiconductor integrated circuit equipment 1, the oxygen sludge 10 which is a gettering field is formed in the semi-conductor support substrate 2 which is the 1st semi-conductor substrate. In order to form the substrate for semiconductor integrated circuits by sticking the bond wafer 9 which is the 2nd semi-conductor substrate created independently, The effect of the surface silicon layer 4 received with the formation process of the oxygen sludge 10 can be avoided, consequently the engine performance of semiconductor integrated circuit equipment 1 can be improved.

[0054] Moreover, since the precipitation-of-oxygen nucleus 7 and the 2nd semi-conductor

substrate containing the surface silicon layer 4 can be manufactured independently, optimization of the process conditions for raising the consistency of the precipitation-of-oxygen nucleus 7 can be attained, without taking into consideration physical-properties change of the 2nd semi-conductor substrate.

[0055] (Gestalt 2 of operation) Drawing 8 is the important section sectional view having shown an example of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.

[0056] The semiconductor integrated circuit equipment 12 of the gestalt 2 of this operation does not have the SOI structure which consists of a surface silicon layer 4 which is a semi-conductor thin film layer formed on BOX3 and BOX3 which are the insulating layer formed on the semi-conductor support substrate 13 and the semi-conductor support substrate 13, and although not illustrated in the surface silicon layer 4, the semiconductor integrated circuit component is formed.

[0057] Moreover, the polycrystal silicone film 14 is formed in the rear face of the semi-conductor support substrate 13 by the thickness which is about 1 micrometer. This polycrystal silicone film 14 serves as a gettering field.

[0058] According to such semiconductor integrated circuit equipment 12, by carrying out gettering of the impurity which exists in the surface silicon layer 4 to the polycrystal silicone film 14 through BOX3 and the semi-conductor support substrate 13, the engine performance of the semiconductor integrated circuit component formed in the surface silicon layer 4 can be improved, and high-performance-izing of semiconductor integrated circuit equipment 12 and improvement in the yield can be aimed at.

[0059] Next, the manufacture approach of the semiconductor integrated circuit equipment 12 of the gestalt 2 this operation is explained according to drawing 9 - drawing 11 .

[0060] First, the silicon wafer 15 which is the 2nd semi-conductor substrate is prepared, a silicon wafer 15 is oxidized thermally, and BOX3 with a thickness of 500nm is formed in a front face (drawing 9). A silicon wafer 15 turns into a near bond wafer with which the component of a SOI wafer is formed.

[0061] The crystal property of a silicon wafer 15 can be made into 550 micrometers in field bearing (100), electric conduction form N type, resistivity 10 ohm-cm, the diameter of 125mm, and thickness.

[0062] Next, the silicon wafer 16 which has the same crystal property as a silicon wafer 15 is prepared, after making a mirror plane side counter mutually and piling up a silicon wafer 15 and a silicon wafer 16, in N2 ambient atmosphere, annealing is performed using the processing time as 3 hours using temperature as 1050 degrees C, both are pasted up firmly, and the lamination wafer 17 is obtained (drawing 10 R> 0). A silicon wafer 16 serves as the semi-conductor support substrate 13.

[0063] Next, it deposits on both sides of the lamination wafer 17 until it becomes the thickness of about 1 micrometer about the polycrystal silicone film 14 using a well-known CVD method (drawing 11).

[0064] next, the field by the side of the silicon wafer 15 of the lamination wafer 17 -- up to thickness thicker [10 micrometers of numbers] than the thickness of the surface silicon layer 4 predetermined with a surface grinder -- removing -- after that -- the chemical mechanical grinding method -- the thickness (for example, 2 micrometers) of the predetermined surface silicon layer 4 -- until -- it grinds. Thus, the substrate for semiconductor integrated circuits which has the polycrystal silicone film 14 used as a

gettering field is formed in the rear face of the semi-conductor support substrate 13.
[0065] Finally a semiconductor integrated circuit component is formed in the front face of the surface silicon layer 4 using a well-known technique, and the semiconductor integrated circuit equipment 12 shown in drawing 8 is completed.
[0066] Since according to the manufacture approach of such semiconductor integrated circuit equipment 12 the polycrystal silicone film 14 is formed after sticking a silicon wafer 15 and a silicon wafer 16, a production process can be simplified. That is, since the direction in which the polycrystal silicone film 14 is formed does not need to remove before lamination the contamination generated at the time of thin film formation forming the polycrystal silicone film 14 beforehand and sticking on the silicon wafer 16 side which is the 1st semi-conductor substrate with a silicon wafer 15 after sticking, a process can be simplified and it is advantageous.
[0067] In addition, although the gestalt 2 of this operation showed the example of the polycrystal silicone film 14 as a gettering field, you may be formation of a silicon nitride film, or surface roughening processing by sandblasting. In this case, an impurity is efficient and gettering of the gettering of an impurity is carried out by generating of the space [distortion] by the interface of the silicon nitride film and the semi-conductor support substrate 13 which were formed, or the roughened stress of a field. Moreover, since these processings are generally processed by whenever [low-temperature], it is rare to affect a device property. In addition, the ambient atmosphere which forms the lamination wafer 17 in this case is N2. Otherwise, it can consider as oxygen. When such, an oxygen induction stacking fault is formed in a mechanical defective part, and the effectiveness of gettering can be raised further.
[0068] Moreover, as an example of the gettering field aiming at generating of mechanical stress, although the example of a silicon nitride film was shown, you may be thin films, such as a carbonization silicone film, aluminum oxide film, and titanium nitride.
[0069] (Gestalt 3 of operation) Drawing 12 is the important section sectional view having shown an example of the semiconductor integrated circuit equipment of this invention which is the gestalt of other operations further.
[0070] The semiconductor integrated circuit equipment 18 of the gestalt 3 of this operation does not have the SOI structure which consists of a surface silicon layer 4 which is a semi-conductor thin film layer formed on BOX3 and BOX3 which are the insulating layer formed on the semi-conductor support substrate 13 and the semi-conductor support substrate 13, and although not illustrated in the surface silicon layer 4, the semiconductor integrated circuit component is formed.
[0071] Moreover, the impurity diffused layer 19 by which Lynn (P) was introduced into high concentration is formed in the interface of the semi-conductor support substrate 13 and BOX3. This impurity diffused layer 19 serves as a gettering field.
[0072] According to such semiconductor integrated circuit equipment 18, by carrying out gettering of the impurity which exists in the surface silicon layer 4 to an impurity diffused layer 19 through BOX3, the engine performance of the semiconductor integrated circuit component formed in the surface silicon layer 4 can be improved, and high-performance-izing of semiconductor integrated circuit equipment 18 and improvement in the yield can be aimed at.
[0073] Next, the manufacture approach of the semiconductor integrated circuit equipment 18 of the gestalt 3 this operation is explained according to drawing 13 - drawing 15 .

[0074] First, the silicon wafer 13 which is the 1st semi-conductor substrate is prepared (drawing 13).

[0075] The crystal property of a silicon wafer 13 can be made into 550 micrometers in field bearing (100), electric conduction form N type, resistivity 10 ohm-cm, the diameter of 125mm, and thickness.

[0076] Next, an impurity diffused layer 19 is formed by doping Lynn (P) to the mirror plane side of a silicon wafer 13 (drawing 14).

[0077] A thermal diffusion method can be used for the approach of doping Lynn (P). In this case, POCl3 The Lynn concentration is abbreviation 1x1021 atom / cm3 by making it the diffusion source and depositing for 15 minutes at 950 degrees C. A phosphorus glass layer is formed and it is N2. 1000 degrees C and annealing for 30 minutes are performed in an ambient atmosphere, and they are a depth of 1 micrometer, concentration 1x1020 atom / cm3. The Lynn diffusion layer can be formed.

[0078] Moreover, ion-implantation can be illustrated as an approach of doping Lynn (P). In this case, P+ They are energy 100keV, and dose 1x1016 ion / cm2 about ion. N2 after pouring in 1000 degrees C and annealing for 30 minutes are performed in an ambient atmosphere, and they are a depth of 1 micrometer, concentration 1x1020 atom / cm3. The Lynn diffusion layer can be formed.

[0079] Next, the silicon wafer 8 explained with the gestalt 1 of operation is prepared, BOX3 is formed in this front face, and the bond wafer 9 is formed (drawing 5). Since it is the same as that of the gestalt 1 of operation about a silicon wafer 8, BOX3, and the bond wafer 9, explanation is omitted.

[0080] Next, N2 after making a mirror plane side counter mutually and piling up a silicon wafer 13 and the bond wafer 9 1050 degrees C and annealing of 3 hours are performed in an ambient atmosphere, both are pasted up firmly, and the lamination wafer 21 is obtained (drawing 1515).

[0081] next, the field by the side of the bond wafer 9 of the lamination wafer 21 -- up to thickness thicker [10 micrometers of numbers] than the thickness of the surface silicon layer 4 predetermined with a surface grinder -- removing -- after that -- the chemical mechanical grinding method -- the thickness (for example, 2 micrometers) of the predetermined surface silicon layer 4 -- until -- it grinds. Thus, the substrate for semiconductor integrated circuits which has the impurity diffused layer 19 used as a gettering field in the interface of the semi-conductor support substrate 13 and BOX3 is formed.

[0082] Finally a semiconductor integrated circuit component is formed in the front face of the surface silicon layer 4 using a well-known technique, and the semiconductor integrated circuit equipment 18 shown in drawing 12 is completed.

[0083] In order according to the manufacture approach of such semiconductor integrated circuit equipment 18 to dissociate and to perform formation of an impurity diffused layer 19 used as a gettering field, and formation of the bond wafer 9 which has the surface silicon layer 4 which influences the engine performance of semiconductor integrated circuit equipment, and BOX3, the physical properties of the surface silicon layer 4 and the interface of BOX3 are not influenced by formation of an impurity diffused layer 19. For example, after forming BOX3, although an impurity may be generated for the residual of the impurity atom within BOX3 introduced etc. through BOX3 thermal diffusion or when

carrying out ion doping, such fault is not produced by the manufacture approach of the gestalt 3 this operation. Consequently, it can contribute to the improvement in the engine performance of semiconductor integrated circuit equipment, and the improvement in the yield.

[0084] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.

[0085]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.

[0086] (1) It became applicable [the gettering technique to the lamination SOI wafer considered to be conventionally difficult]. Namely, embedding SiO2 which is an insulating layer By establishing a gettering field in the semi-conductor support substrate of the membranous lower part, the trap of the contamination heavy metal which enters in the production process of a semiconductor device can be carried out to these gettering fields, and it becomes possible to aim at improvement in the electrical property of a component, and a probe yield. Moreover, since the gettering field was established in the semi-conductor support substrate, it is not necessary to establish a gettering field in the semi-conductor thin film layer prepared on the insulating layer, and the engine performance of the semiconductor integrated circuit component formed in the semi-conductor thin film layer can be improved.

[0087] (2) By using a gettering field as the oxygen sludge distributed over the whole semi-conductor support substrate, the engine performance of a semiconductor integrated circuit component can be improved. Moreover, it can become possible [a semi-conductor thin film layer] to dissociate and to form a gettering field, it is not necessary to form a denuded zone in a semi-conductor thin film layer, and a production process can be simplified by establishing the gettering field which consists of an oxygen sludge in the semi-conductor support substrate instead of a semi-conductor thin film layer.

[0088] (3) Since the impurity diffused layer into which high-concentration Lynn (P) was introduced was prepared, gettering of the metal impurity can be carried out according to the chemical operation by increase of ****** of a metallic element.

[0089] (4) Since it forms by the thin film or stress generating field in which the gettering field was established at the rear face of a semi-conductor support substrate, it becomes the structure which added the gettering field to the substrate for semiconductor integrated circuits which does not have a gettering field, and a gettering field can be formed comparatively freely in the phase of the arbitration of the production process of semiconductor integrated circuit equipment. Thereby, it becomes easy to attain optimization of the whole production process of semiconductor integrated circuit equipment.

[0090] (5) In order to use as a polish recon thin film or a silicon nitride film the thin film which is a gettering field, or since a gettering field is formed by surface roughening processing by the collision of the particle injected by the rear face, gettering of a metal impurity can be performed effectively and the engine performance of semiconductor integrated circuit equipment can be improved.

[0091] (6) Since a gettering field is formed in the 1st semi-conductor substrate and the

substrate for semiconductor integrated circuits is formed by sticking with the 2nd semi-conductor substrate created independently, it can hold good, without degrading the quality of the semi-conductor thin film layer which can avoid the effect on the semi-conductor thin film layer received by the production process of a gettering field, consequently influences the engine performance of a semiconductor integrated circuit component by the production process of a gettering field.

[0092] (7) An oxygen sludge or the process conditions of manufacture of an impurity diffused layer can be optimized, without being able to manufacture apart from the 2nd semi-conductor substrate containing the semi-conductor thin film layer which influences the engine performance of a semiconductor integrated circuit component in an oxygen sludge or an impurity diffused layer, and taking into consideration physical-properties change of the 2nd semi-conductor substrate.

[0093] (8) Since a gettering field is formed after sticking the 1st semi-conductor substrate and the 2nd semi-conductor substrate, a production process can be simplified.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the important section sectional view having shown an example of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 2] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 3] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 4] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 5] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 6] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 7] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 8] It is the important section sectional view having shown an example of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.

[Drawing 9] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.

[Drawing 10] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.

[Drawing 11] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.

[Drawing 12] It is the important section sectional view having shown an example of the semiconductor integrated circuit equipment of this invention which is the gestalt of other operations further.

[Drawing 13] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment of this invention which is the gestalt of other operations further.

[Drawing 14] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment of this invention

which is the gestalt of other operations further.

[Drawing 15] It is the important section sectional view having shown an example of the production process of the semiconductor integrated circuit equipment of this invention which is the gestalt of other operations further.

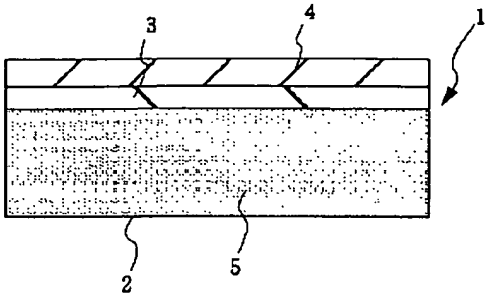
[Description of Notations]

1 12 Semiconductor integrated circuit equipment
2 13 Semi-conductor support substrate
3 BOX
4 Surface Silicon Layer
5 Oxygen Sludge
6, 8, 15, 16 Silicon wafer
7 Precipitation-of-Oxygen Nucleus
9 Bond Wafer
10 Oxygen Sludge
11 Lamination Wafer
14 Polycrystal Silicone Film
17 21 Lamination wafer
18 Semiconductor Integrated Circuit Equipment
19 Impurity Diffused Layer

DRAWINGS

[Drawing 1]

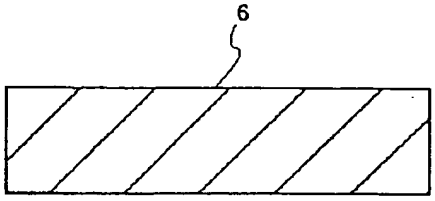
図 1



1 半導体集積回路装置
2 半導体支持基板
3 BOX
4 表面シリコン層
5 酸素析出物

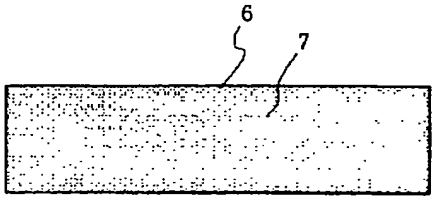
[Drawing 2]

図 2



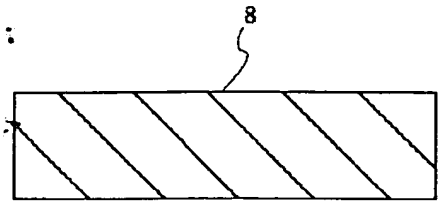
[Drawing 3]

図 3



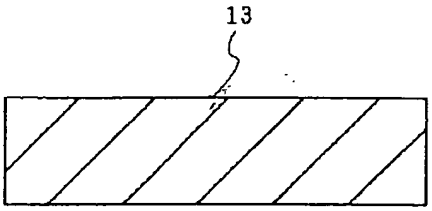
[Drawing 4]

図 4



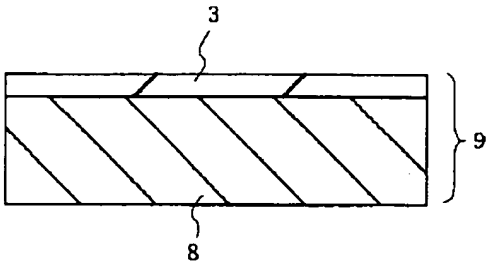
[Drawing 13]

図 13



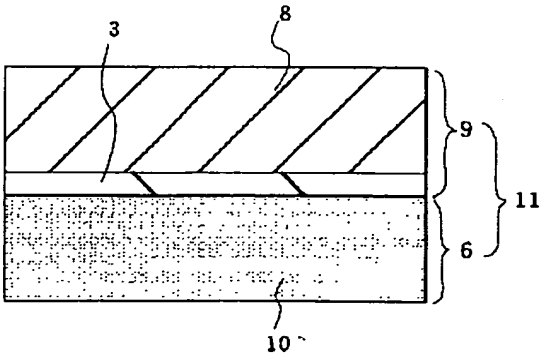
[Drawing 5]

図 5



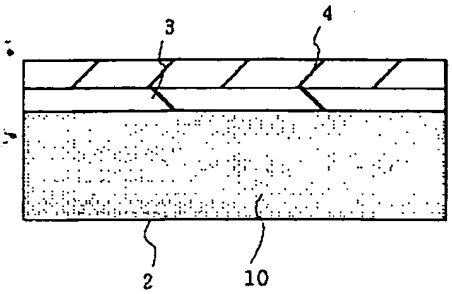
[Drawing 6]

図 6



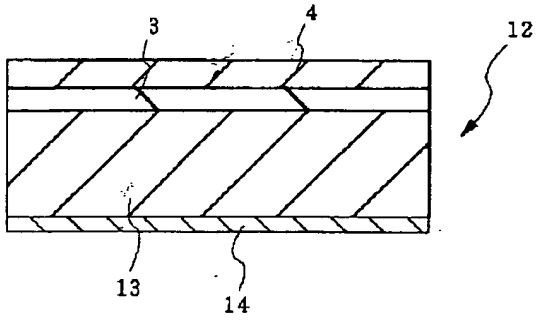
[Drawing 7]

図 7



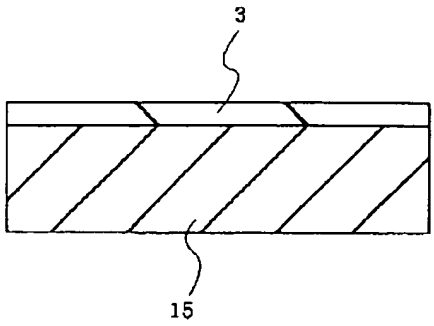
[Drawing 8]

図 8



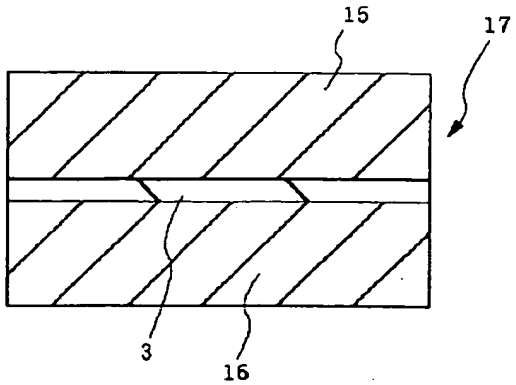
[Drawing 9]

図 9



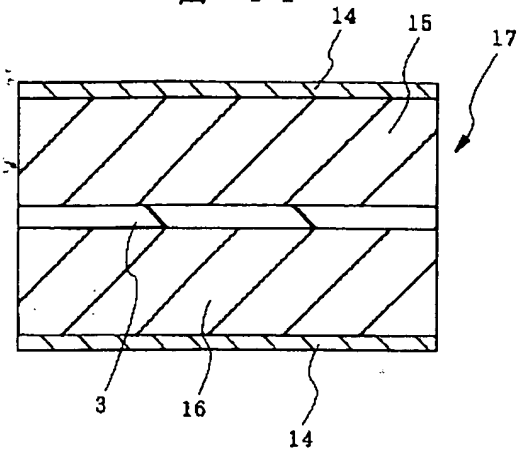
[Drawing 10]

図 10



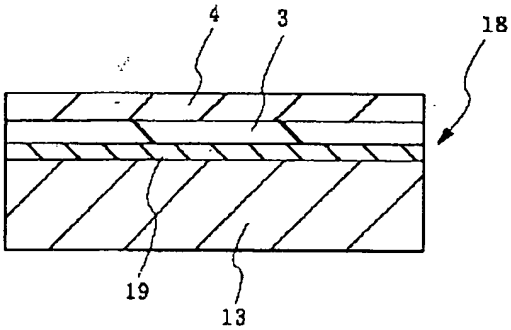
[Drawing 11]

図 11



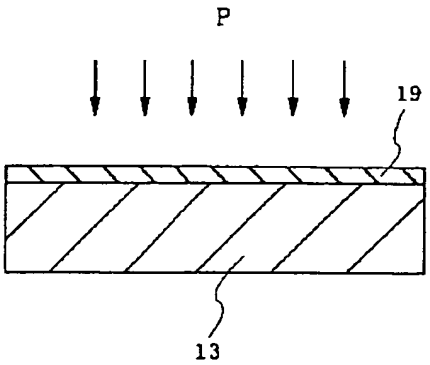
[Drawing 12]

図 12



[Drawing 14]

図 14



[Drawing 15]

図 15